International Summer School on Digital Chip Design

RISC-V on a chip in three days

June 10th to 12th, 2025 at Lund University, Sweden

The summer school is organized by Senior Advisor Per Andersson, PhD, Lund University.

Dr Andersson's main interests are in design of digital IC:s. He has a background as researcher, lecturer and entrepreneur and is now responsible for, and currently developing, the Batchelor level courses in digital design and computer organization at Lund University. This includes using open-source tools to implement a RISC-V design on FPGA during the laboratory work of the introductory course in digital design given in the sophomore year on the EE and CE programs.

Abstract

You will design your own, simple RISC-V processor from scratch to executing programs in hardware within the timeframe of this three-day summer school. Key take-aways include overview of modern digital chip design, insight into the RISC-V architecture, as well as insight into the incredible, combined power and simplicity of open-source tools applied to a non-trivial design. Although the designs could, in principle, be fabricated as standard CMOS chips, we will use Field-Programmable devices to avoid a multi-month wait and a huge cost.

Background

Are you curious about how a computer really works? For programs to run on more than one computer, they need to be standardized. We will focus on RISC-V, which is uniquely not owned by any computer chip manufacturer.

Computers are built from chips performing simple instructions. To really understand what's going on we investigate how these chips are created.

During the summer school, we will create our own physical version of a computer chip. It will be realized in an FPGA allowing a lot of existing, simple building blocks to be hooked up to your liking. We will work together to complete the design of a fully working computer, capable of running real programs, in three days.

Starting at arrival night and throughout the summer school we will include outings, connect to local industry, and generally have a good time.

Audience

The summer school is directed to anyone interested in digital chip design, RISC-V and the power and simplicity of present generation open-source tools. No prior experience in the field is expected or required, but basic skills in programming and math is highly recommended. We will focus on how digital systems capable of executing real programs

can be integrated with ease and thereby inspire and encourage the next generation of engineers to exploit and implement such functionality in their future designs.

Program

The summer school is given on-site at the Department of Electrical and Information Technology, Klas Anshelms väg 10, Lund, Sweden. To find us easy use the map at https://summerschool.eit.lth.se/.

There will be a welcoming event at the department on Monday, June 9th at 17.00, especially for those travelling to Lund.

Throughout the three day the schedule will start with a common tutorial/lecture at 9.00 for about 90 minutes. With a break for lunch, we will then spend until 16.00 in our labs under the guidance of our experienced teaching assistants and faculty.

In the early evenings of Tuesday and Wednesday we organize joint activities to summarize the day, learn from each other and have fun. One night will include a visit to a company visit to learn about their use of digital, in-house designed chips.

Pre-requisites

One point of the summer school is to demonstrate the ease of use emerging from delivering the tools into, and executing them inside, the user's web browser without installation or downloads. Thus, the summer school can be followed in full using no other pre-requisites than a (reasonably modern) web browser running on a laptop. FPGA-boards needed are provided in our labs.

We use well-known, open-source tools, such as Yosys and Verilator, using our own integration for delivery and use across the web.

Participation

See https://summerschool.eit.lth.se/ for a link to sign up.

The summer school is free, but travel and accommodation must be arranged and covered by the participants. We do not have any travel grants to offer.

Acknowledgements

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